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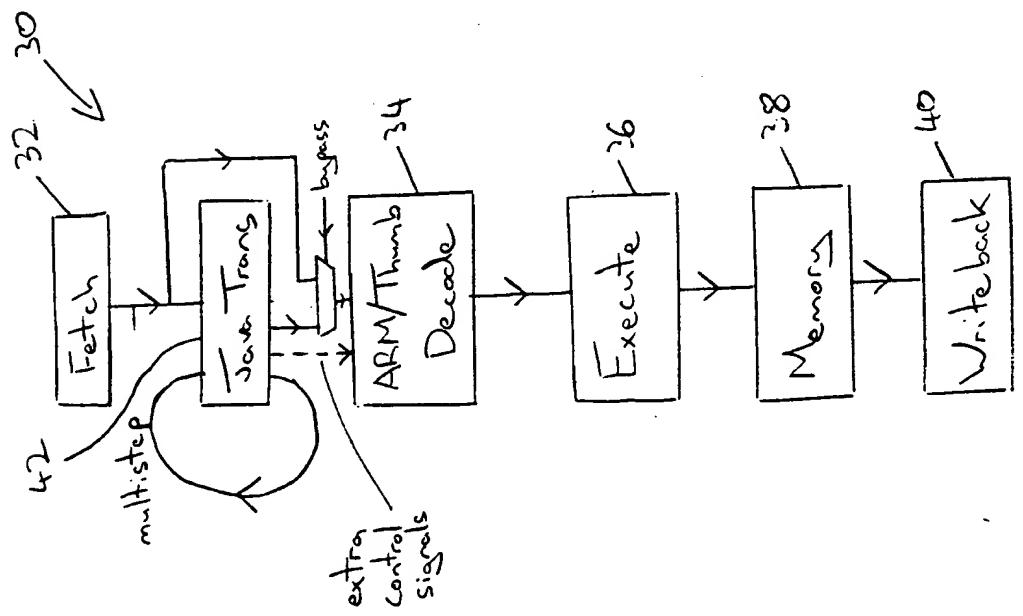


Fig. 1

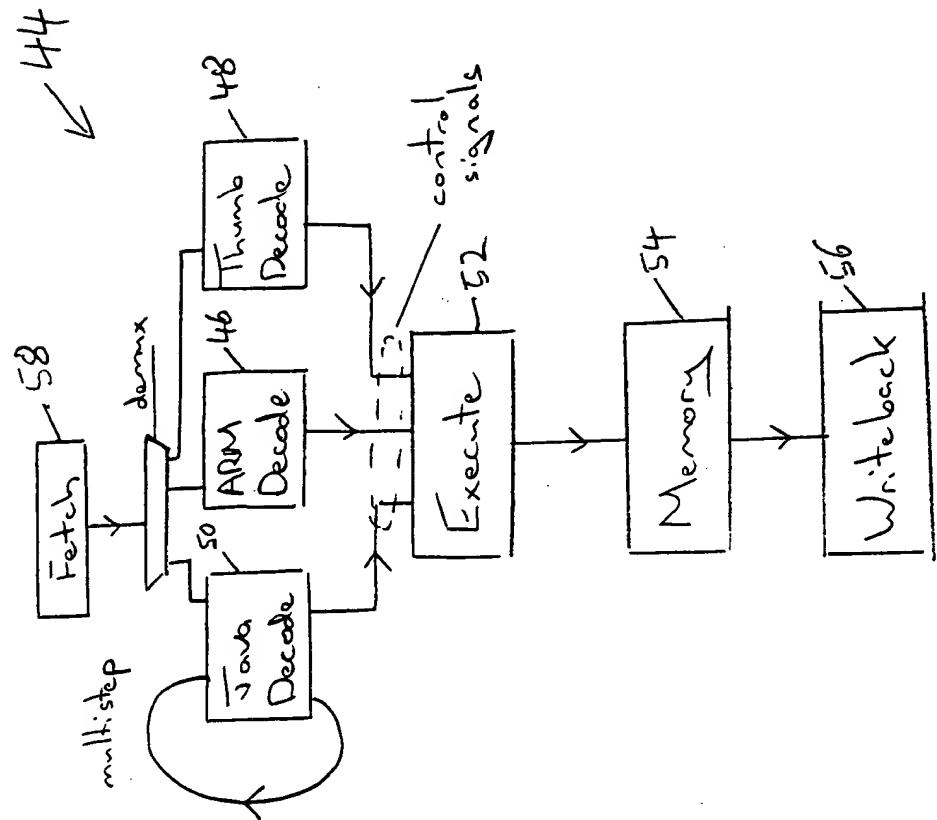


Fig. 2

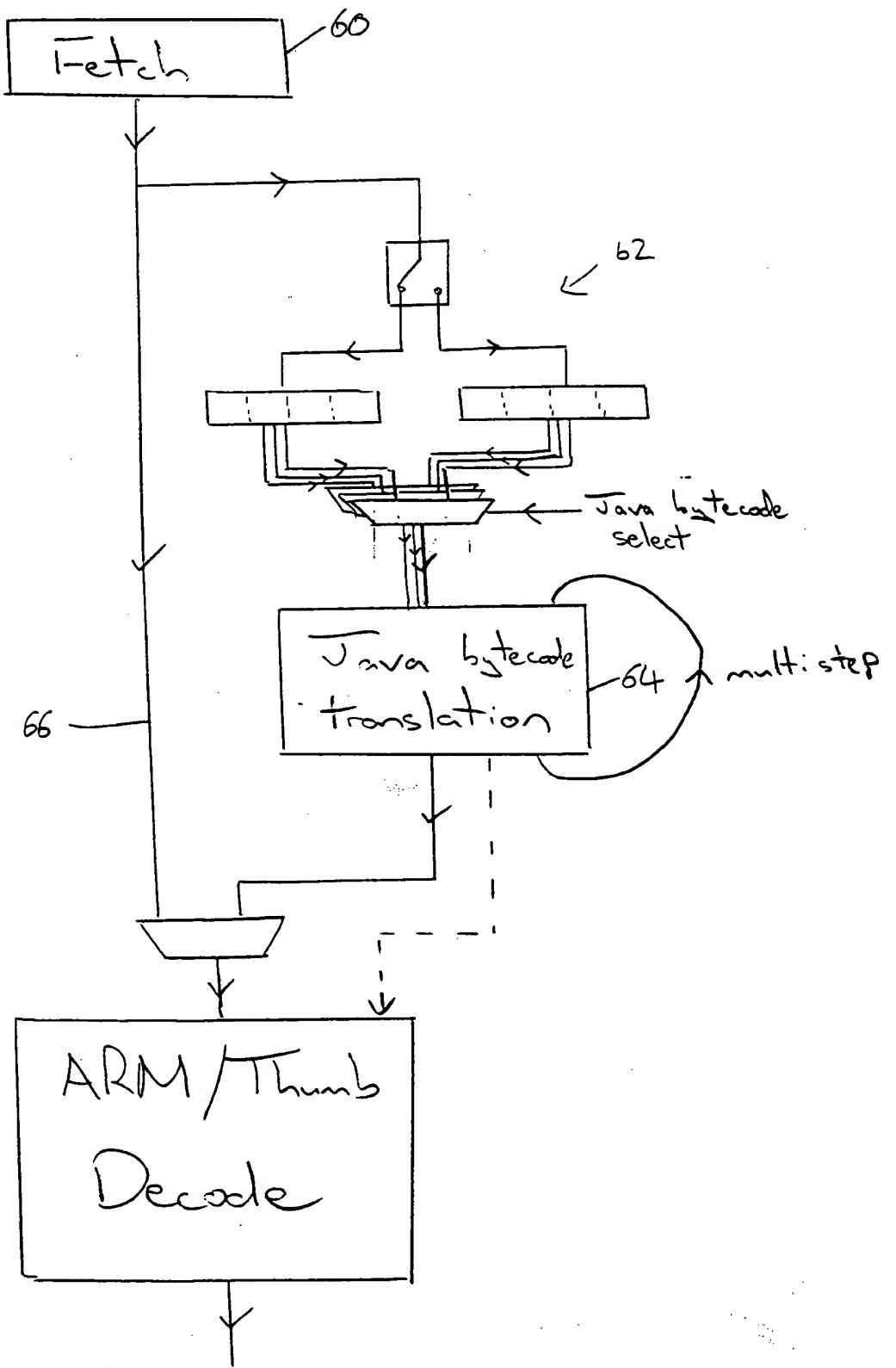


Fig. 3

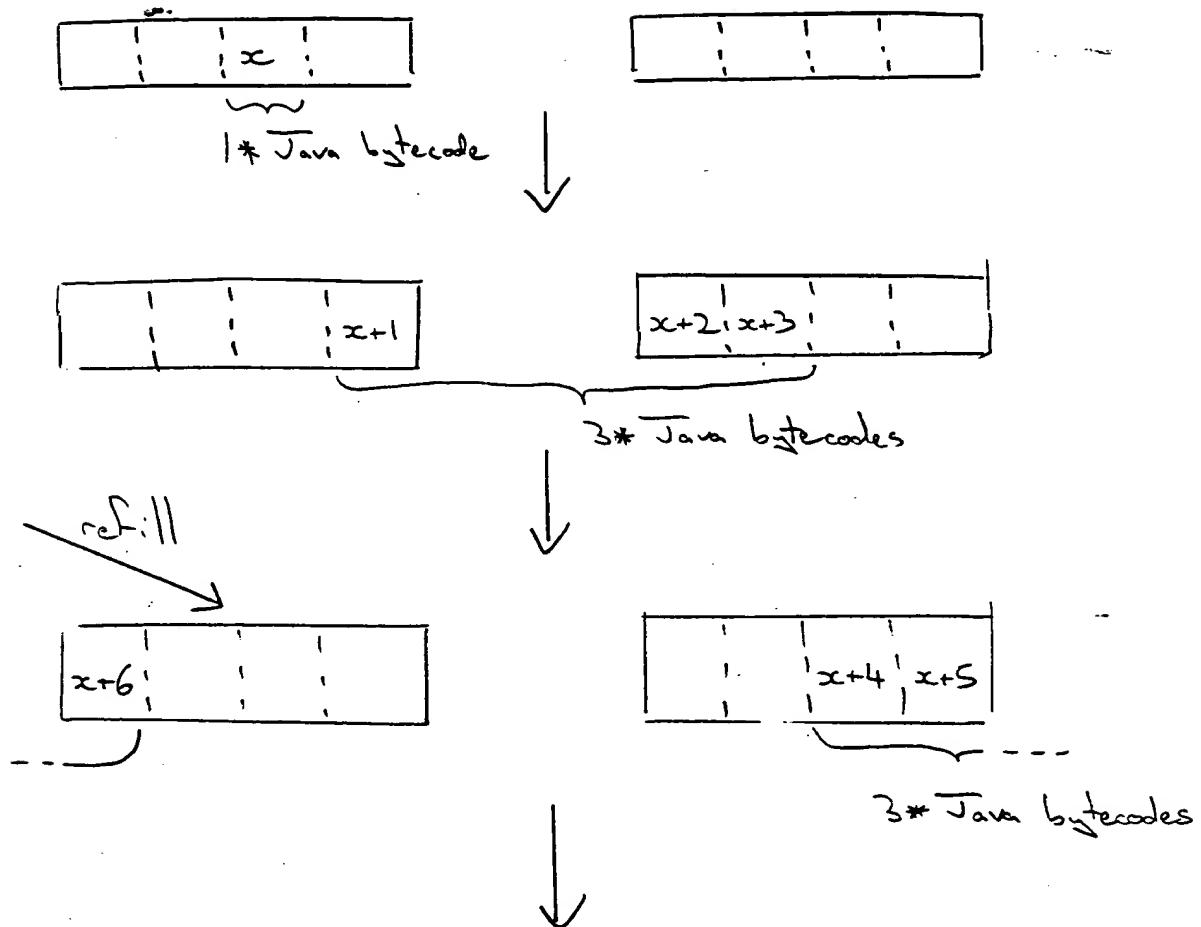


Fig. 4

$10^2$

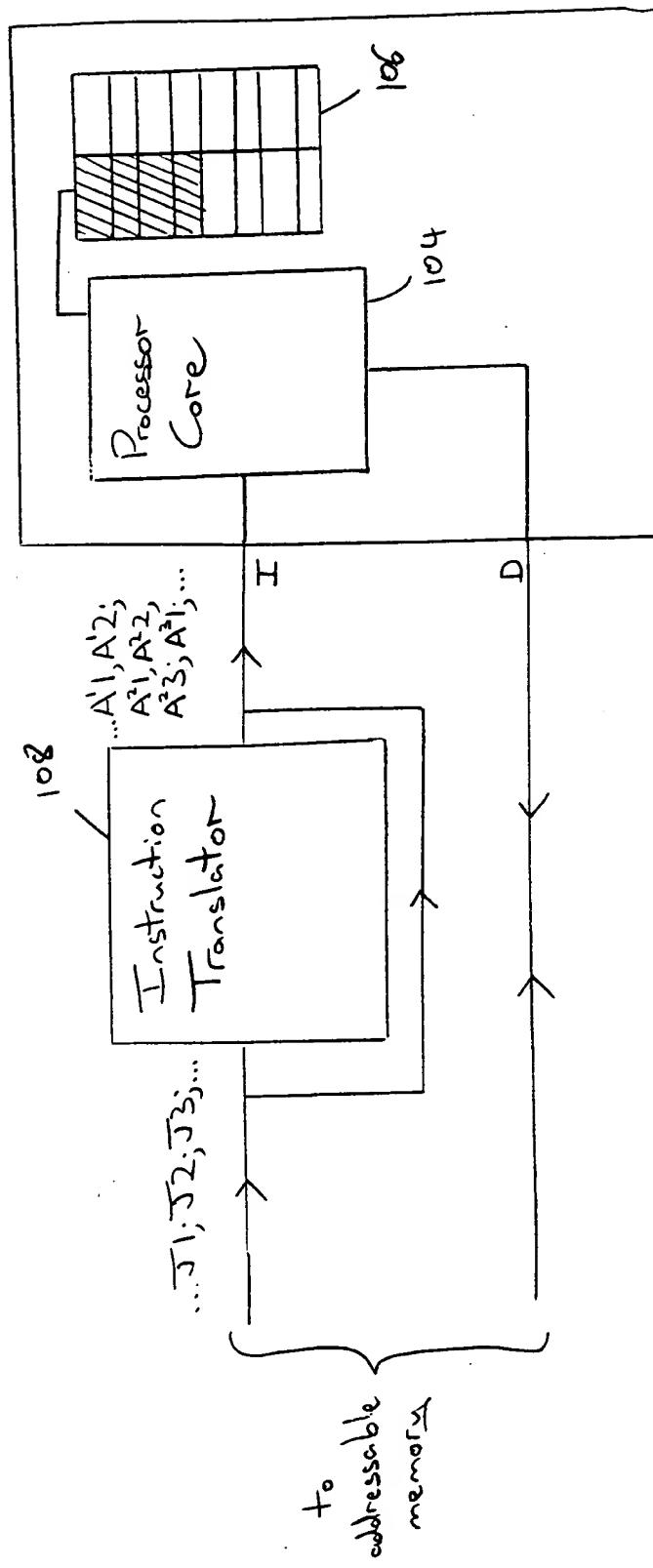
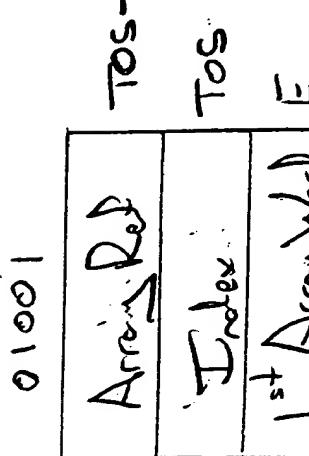
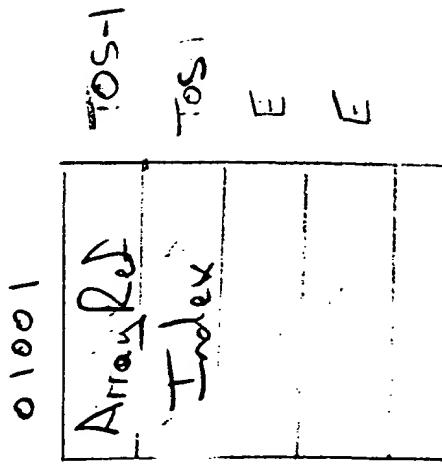


Fig. 5

Fig. 6.

$\frac{0 \text{ load}}{\text{RF} = 2}$       SA = 0  
 $\text{RE} = 2$       (swap)



LDR R12,[R0,#0]  
 LDR R2,[R2,R1],LSL#3]

E

01001

TOS  
 TOS

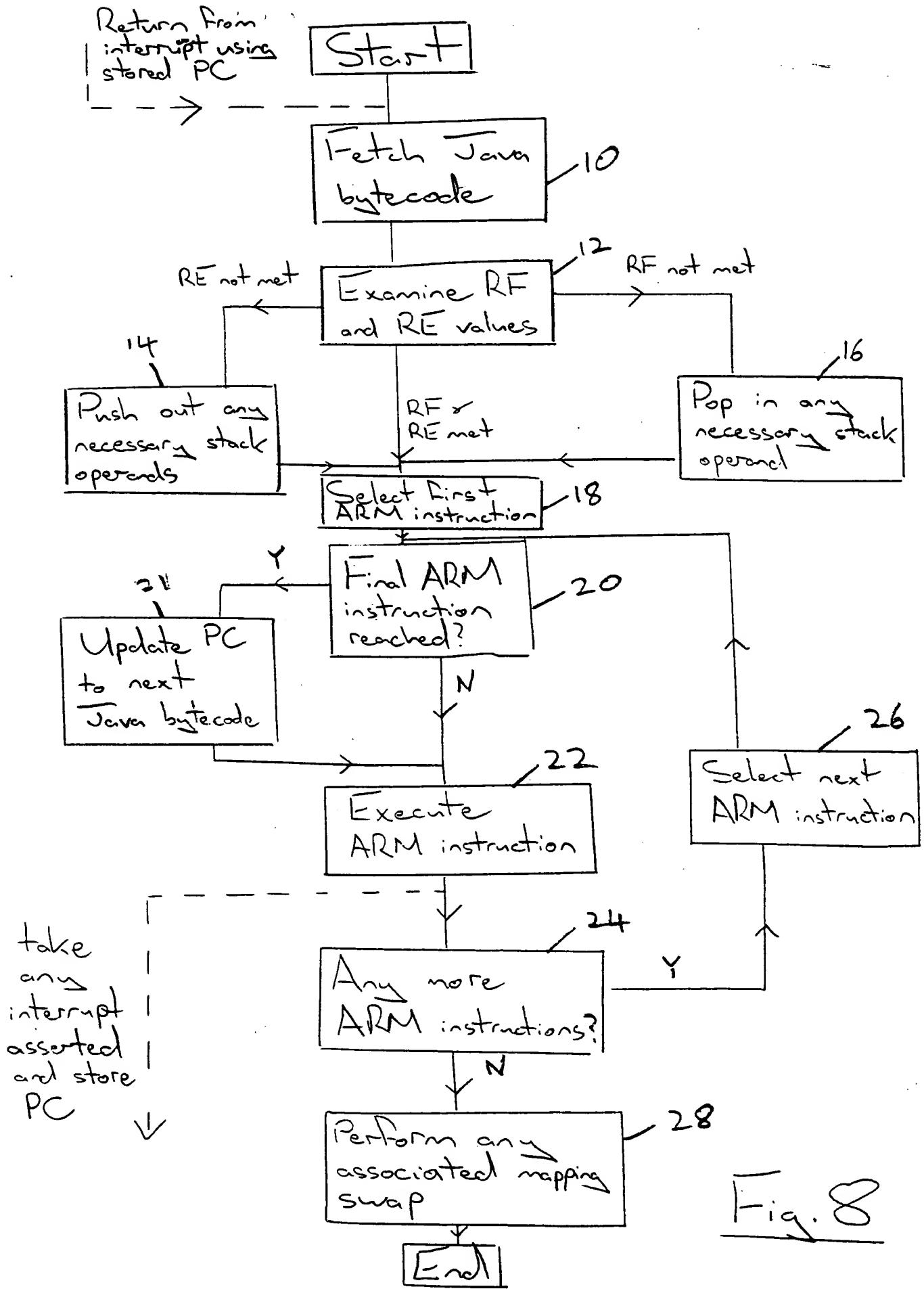
TOS  
 TOS



01011

LDR R3,[R12,#4]  
 (state swap)

Fig. 7



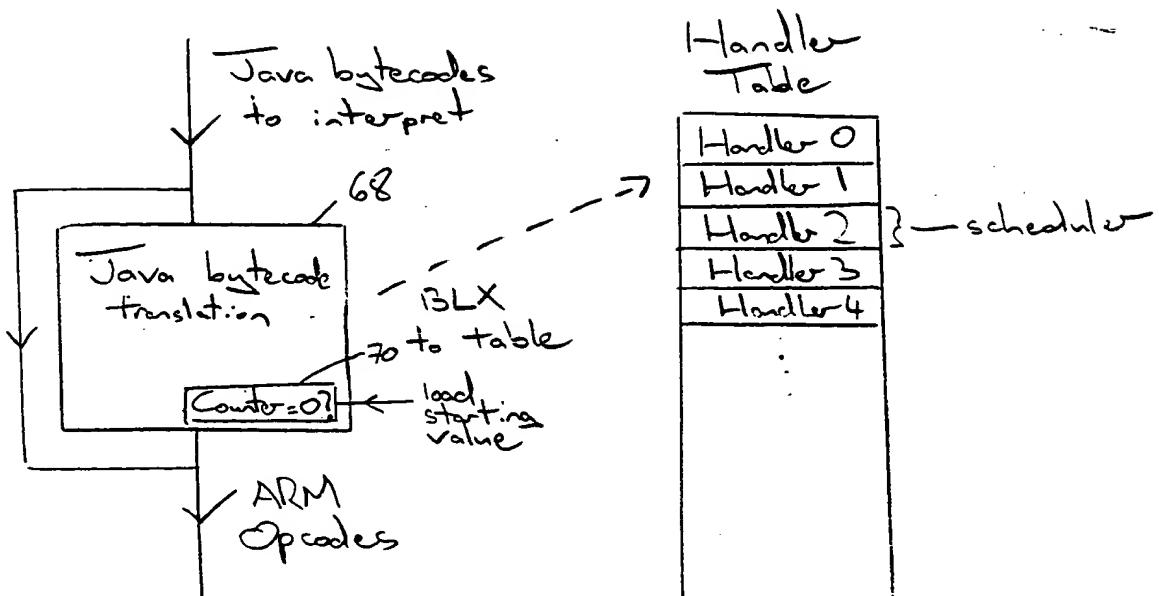


Fig. 9

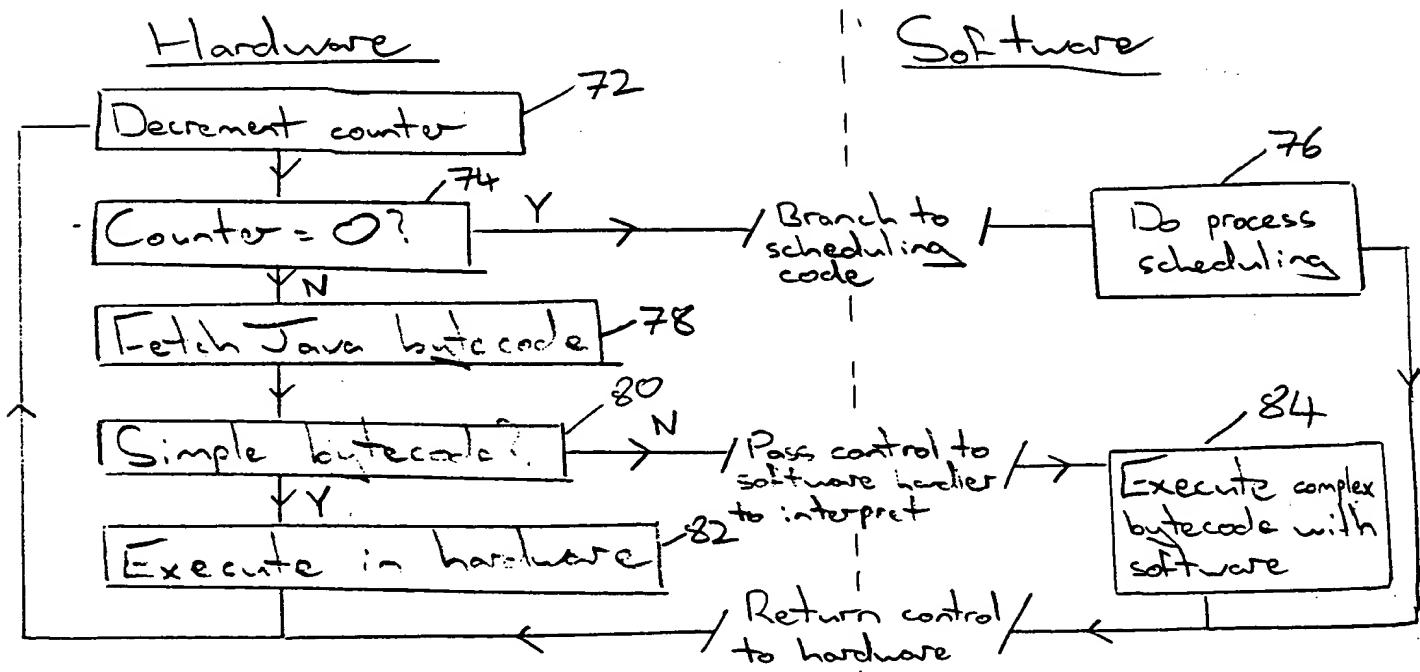
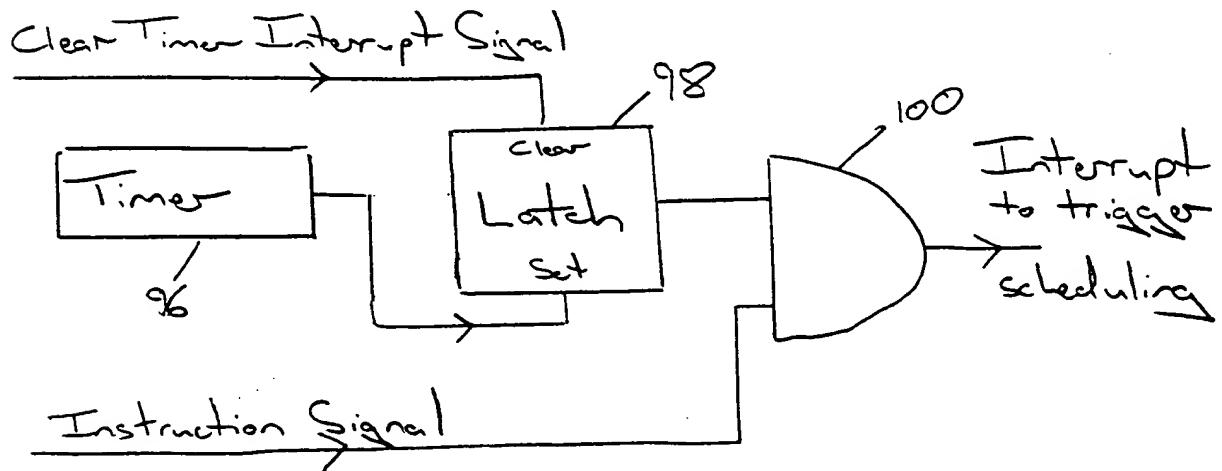
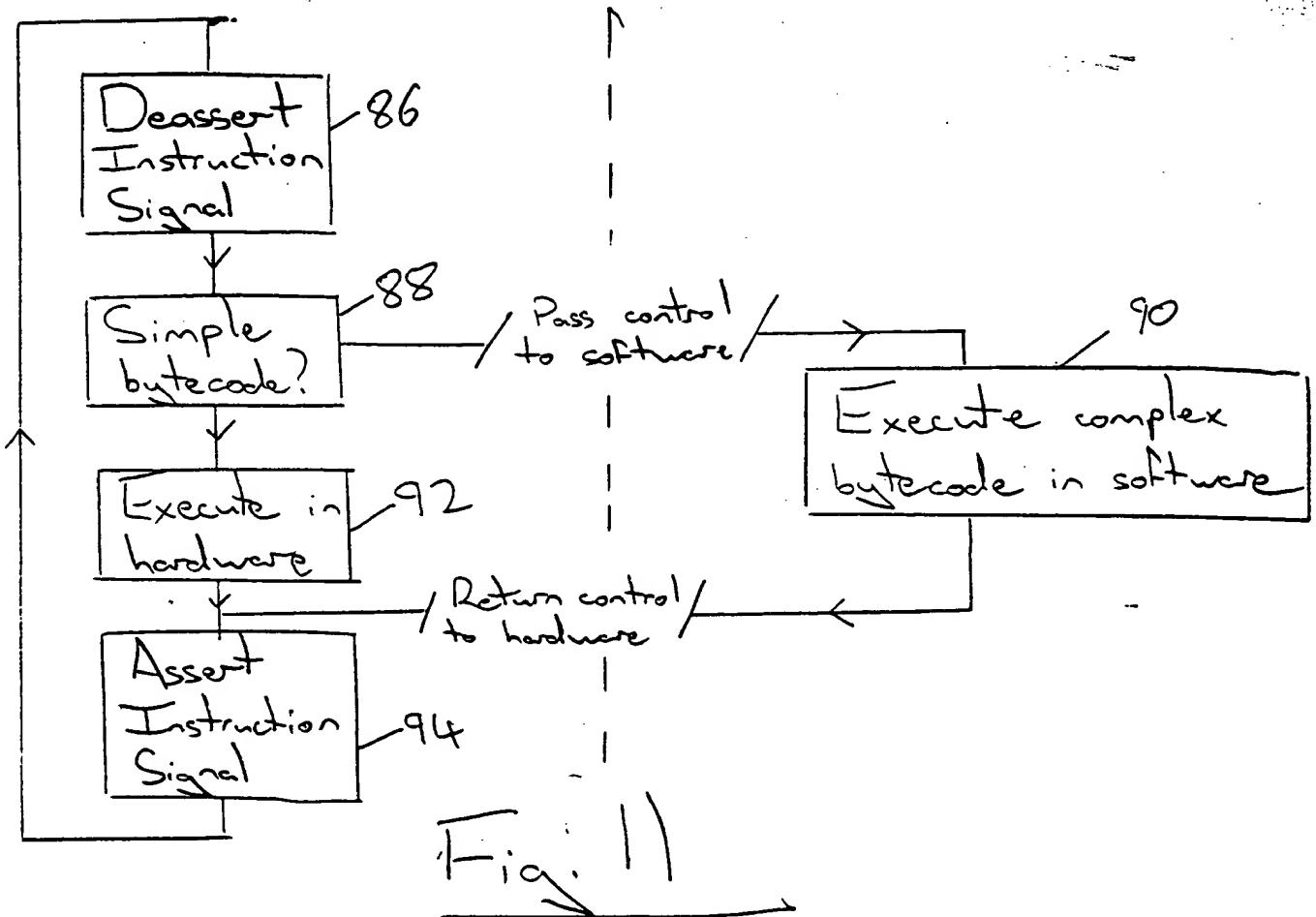


Fig. 10

## Hardware

## Software





Core  
Clock



Timer



Latched  
Timer



Instruction



Interrupt



Clear  
Interrupt

Fig. 13